

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,867,483 B2
APPLICATION NO. : 09/909934
DATED : March 15, 2005
INVENTOR(S) : Huat et al.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4: Claims 1-14 should read as follows:

1. A ~~stress-free~~ lead frame comprising;
a plurality of integrated circuit areas, each of said plurality of integrated circuit areas having a die pad and a plurality of leads; and
a peripheral pad surrounding said plurality of integrated circuit areas, the peripheral pad comprising first and second parallel opposing support bars and third and fourth parallel opposing support bars arranged orthogonal to the first and second opposing support bars;
said peripheral pad being provided with a plurality of stress-relief openings alone each of the first, second, third and fourth support bars.

2. A ~~stress-free~~ lead frame as claimed in claim 1 wherein the peripheral pad further comprises:
a plurality of interlocking means along the first, second, third and fourth support bars.

3. A ~~stress-free~~ lead frame as claimed in claim 1 wherein said plurality of stress-relief openings comprises holes and slots, each hole being a non-elongated opening and each slot being an elongated opening.

4. A ~~stress-free~~ lead frame as claimed in claim 3 wherein said holes and slots are arranged in multiple rows.

5. A ~~stress-free~~ lead frame as claimed in claim 2 wherein each of said interlocking means comprises a plurality of slots, each slot being an elongated opening.

6. A ~~stress-free~~ lead frame as claimed in claim 4 wherein said holes and slots are arranged side by side at equal intervals.

7. A ~~stress-free~~ lead frame as claimed in claim 5 wherein said holes and slots are arranged side by side at equal intervals.

8. The ~~stress-free~~ lead frame as claimed in claim 1 wherein the peripheral pad further comprises a plurality of positioning holes on the first and second support bars.

9. A lead frame strip for use in making an integrated circuit die package, the lead frame strip comprising:
an outer frame having a plurality of elongated stress relief openings around the circumference of the outer frame;
a plurality of horizontal and vertical connecting bars attached to the other frame

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and defining a plurality of inner frames arranged in a matrix pattern within the outer frame, each inner frame comprising a die pad and a plurality of tabs arranged around the die pad.

10. The lead frame of claim 9 wherein the outer frame further comprises a plurality of non-elongated holes around the circumference of the outer frame.

11. The lead frame of claim 9 wherein the outer frame comprises a plurality of rows of elongated openings around the circumference of the outer frame.

12. The lead frame of claim 11 wherein the outer frame further comprises a plurality of non-elongated holes around the circumference of the outer frame, the non-elongated holes being arranged in a row distinct from the plurality of rows of elongated openings.

13. The lead frame of claim 11 wherein the plurality of elongated openings in at least one of the plurality of rows of elongated openings are regularly spaced along each portion of the outer frame.

14. The lead frame of claim 11 wherein the outer frame comprises at least three rows of elongated openings around the circumference of the outer frame.

Column 4, line 60, after claim 14 insert claims 15-37:

15. The lead frame of claim 14 wherein the three rows of elongated openings comprise a first row, a second row and a third row between the first and second rows, and wherein the first row has a plurality of elongated openings that are substantially the same size and shape as a corresponding plurality of elongated openings in the second row.

16. The lead frame of claim 15 wherein the third row comprises a plurality of elongated openings offset from the plurality of elongated openings in the first and second rows such that it is possible to draw a line orthogonal to the plurality of rows that intersects one of the elongated openings of the third row without intersecting an elongated opening in the first or second rows adjacent to the third row.

17. The lead frame of claim 16 wherein the outer frame further comprises a plurality of non-elongated holes around the circumference of the outer frame, the non-elongated holes being arranged in a row between the first and second rows of elongated openings.

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18. The lead frame of claim 17 wherein the plurality of non-elongated holes are offset from the plurality of elongated openings in the first and second rows such that it is possible to draw a line orthogonal to the plurality of rows that intersects one of the holes without intersecting an elongated opening in the first or second rows adjacent to the third row.

19. The lead frame of claim 9 wherein the outer frame further comprises a plurality of positioning holes located outside the plurality of rows of elongated openings.

20. The lead frame of claim 9 wherein the outer frame has a rectangular shape.

21. A lead frame strip for use in making an integrated circuit die package, the lead frame strip comprising:
an outer frame having a plurality of stress relief openings around the circumference of an inner portion of the outer frame and a plurality of positioning holes along an outer portion of the outer frame;
a plurality of horizontal and vertical connecting bars attached to the outer frame and defining a plurality of inner frames arranged in a matrix pattern within the outer frame, each inner frame comprising a die pad and a plurality of tabs arranged around the die pad.

22. The lead frame strip of claim 21 wherein the plurality of stress relief openings comprise a plurality of rows of openings.

23. The lead frame strip of claim 22 wherein the plurality of rows of openings comprise at least one row comprising a plurality of elongated openings.

24. The lead frame strip of claim 23 wherein the plurality of elongated openings comprise a plurality of regularly spaced elongated openings.

25. The lead frame strip of claim 23 wherein the plurality of rows of openings comprise at least one row comprising a plurality of non-elongated holes.

26. The lead frame strip of claim 25 wherein the plurality of non-elongated holes comprise a plurality of regularly spaced non-elongated holes.

27. The lead frame strip of claim 21 wherein the plurality of stress relief openings comprise a plurality of rows of elongated openings and at least one row of non-elongated holes.

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28. The lead frame strip of claim 27 wherein the plurality of rows of elongated openings comprises a first row and a second row and wherein the first row has a plurality of elongated openings that are offset from the plurality of elongated openings in the second row.

29. The lead frame strip of claim 27 wherein the plurality of rows of elongated openings further comprises a third row and wherein the third row comprises a plurality of elongated openings that are substantially the same size and shape as a corresponding plurality of elongated openings in the first row.

30. The lead frame strip of claim 21 wherein the plurality of stress relief openings comprise at least row of elongated openings that are elongated in the direction of the row.

31. The lead frame strip of any one of claims 21-30 further comprising encapsulant covering the die pad and plurality of tabs within each of the plurality of inner frames and covering the plurality of stress relief openings around the circumference of the inner portion of the outer frame.

[[9]]32. A method of manufacturing a plurality of integrated circuit packages, the method comprising:

providing a lead frame strip comprising (i) an outer frame having a plurality of stress relief openings around a circumference of an inner portion of the outer frame and a plurality of positioning holes along an outer portion of the outer frame, and (ii) a plurality of horizontal and vertical connecting bars attached to the outer frame and arranged in a manner that defines a plurality of inner frames arranged in a matrix pattern within the outer frame, each inner frame comprising a die pad and a plurality of leads arranged around the die pad;

placing an integrated circuit die on each die pad, and for each integrated circuit die, electrically connecting the integrated circuit die to the plurality of leads surrounding its respective die pad;

applying encapsulant material over the lead frame strip so that the plurality of inner frames including each integrated circuit placed on each die pad within the plurality of inner frames and the plurality of stress relief openings are covered by the encapsulant material;

severing individual integrated circuit packages from the lead frame strip to create the plurality of integrated circuit packages.

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[[10]]33. The method of claim [[9]]32 wherein the step of applying encapsulant material comprises heating pellets of encapsulant material placed in a mold to liquefy the material.

[[11]]34. The method of claim [[10]]33 wherein the plurality of stress relief openings comprise a plurality of rows of openings.

[[12]]35. The method of claim [[11]]34 wherein the plurality of rows of openings include a plurality of rows of elongated openings and at least one row of non-elongated holes.

[[13]]36. The method of claim [[11]]34 wherein the plurality of rows of elongated openings comprises a first row and a second row and wherein the first row has a plurality of elongated openings that are offset from the plurality of elongated openings in the second row.

[[14]]37. The method of claim [[12]]35 wherein the plurality of rows of elongated openings further comprises a third row and wherein the third row comprises a plurality of elongated openings that are substantially the same size and shape as a corresponding plurality of elongated openings in the first row.

Signed and Sealed this

Twenty-second Day of July, 2008

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS
Director of the United States Patent and Trademark Office